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(0) (graded near (dielectric insulat$5)) near8 (((back adj gate) backgate (body adj region) (flo...
(0) (graded near (dielectric insulat$5)) with (((back adj gate) backgate (body adj region) (floa...
(15425) (((back adj gate) backgate (body adj region) (float$4 adj (gate electrode) FG)))
(0) (((back adj gate) backgate (body adj region) (float$4 adj (gate electrode) FG)))
(5) (((back adj gate) backgate (body adj region) (float$4 adj (gate electrode) FG)))
(218387) (graded stepped)
(452) ((graded stepped))) near (dielectric insulat$5)
(0) (((graded stepped)))
(0) (((graded stepped)))
(9) (((graded stepped)))
(9) (((graded stepped)))
(4) ("6210999" "6541280").pn.
(141) ((((((barrier adj height) (energy adj band))) near2 (asymmetr$4 differen$2)) and ((float$3...
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((((((barrier adj height) (energy adj band))) near2 (asymmetr$4 differen$2)) and ((float$3 adj gate) and (control adj gate)) ((((((float$3 adj gate) same (control adj gate)) same ((((barrier near (height tunnel)) ((energy diagram) near band))
) (work adj function))) and (metal adj oxide)) ((((float$3 adj gate) same (control adj gate)) and (ald (atomic adj layer adj deposit$3)))))) ((((float$3 control) adj gate intergate) same ((graded stepped) near (composition$4 tunnel$4 concentrat$4))) and ((float$3 control) adj gate intergate))) ((((((perovskite superlattice)
) with ((float$3 control) adj gate intergate)) not "Forbes, Leonard".in.) and ((perovskite superlattice)
) and ((float$3 control) adj gate intergate)) (((transition$3 near metal near2 oxide) and ((float$3 control) adj gate intergate)) not "Forbes, Leonard".in.))

Jan 2004

	U	*	Inventor	Document ID	Issue Date	Page	Title	Current OR	Current XRef
1			Beltram, Fabio et al.	US 4945393 A	19900731	11	Floating gate memory circuit and apparatus	365/185.06	257/316; 257/E29.316;
2			Essaian, Stepan	US 5877977 A	19990302	5	Nonvolatile memory based on metal-ferroelectric-metal-insulator semiconductor structure	365/145	257/E29.272; 257/E29.302;
3			Gardner, Mark I. et al.	US 6210999 B1	20010403	14	Method and test structure for low-temperature integration of high dielectric constant gate dielectrics into self-aligned semiconductor devices	438/183	257/332; 257/E21.209;
4			AHN, K Y et al.	US 20030048666 A	20030313		Floating gate transistor for memory array used in programmable logic array, comprises control gate opposing floating gate, and is separated from floating gate by graded composition		
5			AHN, K Y et al.	US 20030045082 A	20030306		Floating gate transistor for memory modules used in electronic systems, includes control gate separated from floating gate by asymmetrical low tunnel barrier interpoly insulator formed b		
6			AHN, K Y et al.	US 20030042527 A	20030306		Depletion mode floating gate transistor for flash memory, has control gate separated from floating gate by asymmetrical metal oxide made low tunnel barrier interpoly insulator		
7			Ahn, Kie Y. et al.	US 20040004244 A1	20040109		Structures, methods, and systems for ferroelectric memory transistors	257/314	
8			Ahn, Kie Y. et al.	US 20030228747 A1	20031211		Pr2O3-based la-oxide gate dielectrics	438/591	
9			Ahn, Kie Y. et al.	US 20030227033 A1	20031211		Atomic layer-deposited HfA1O3 films for gate dielectrics	257/213	
10			Ahn, Kie Y. et al.	US 20030207540 A1	20031106		ATOMIC LAYER-DEPOSITED LAAlO3 FILMS FOR GATE DIELECTRICS	438/287	438/785
11			Ahn, Kie Y. et al.	US 20020130338 A1	20020919	9	Structures, methods, and systems for ferroelectric memory transistors	257/295	257/E21.208;

Ready